УДК 004.93

V.G. Krasilenko[1], C. Sc.; A.A. Lazarev [1], C. Sc.; D.V. Nikitovich [1]
[1] Vinnytsia National Technical University

A RANK ANALOGUE PRE-PROCESSOR BASED ON ITTERATIVE SORTING NODE FOR IMAGE NONLINEAR PROCESSING

Introduction. The strategic direction becomes fast parallel processing of 1D or 2-D array using non-conventional MIMO-systems, corresponding matrix logics (multi-valued, continuous, neural-fuzzy and others) and corresponding mathematical apparatus. A lot of demonstrator systems were built to prove the use of optics or optoelectronics for off-chip and on-chip interconnects [1]. Optical detectors, photodiodes can be monolithically integrated with digital electronics in silicon, which allows the realization of stacked 3-D chip architecture in principle and significantly simplifies design of OE-VLSI circuits, which in addition should contain only light-emitting devices [2]. Smart optical sensors [3] show a great application field and potential. Therefore our approach favors smart pixel like architecture combining parallel signal detection with parallel signal processing in circuit. Each pixel has its own analog and analog-digit node what guarantees the fastest processing. For perspective realizations of optical learning neural networks (NN) with 2D structure, of the continuously-logic (CL) equivalency models (EM) NN [4, 5], the elements of matrix continuous and threshold logics are required. One directions of research is the application of time-pulse-coded architectures (TPCA) that were considered in works [4, 5]. By the variety and scope of applications in information technology, Boolean two-digit logic covers the entire binary-discrete (virtual) world and therefore the 20th century can rightly be called Boolean. But in the majority of cases, various production processes and technologies are accompanied not by discrete, but by accompanying continuous analog processes and signals, which leads to contradictions in the use of discrete logics in the continuum. Therefore, for the description and modeling of each continual subject domain and the class of its tasks, its own logical-algebraic apparatus is required. Logic-algebraic (LA) calculi are mathematical (symbolic) domain-oriented logics and special algebras, the formal apparatus of which is based on clear rules that allow you to make an exact description of a certain class of problems and even suggest an algorithm for solving them. For the successful development of continual information technologies and artificial intelligence [6], it is necessary to increase the semantic power of LA-calculus. The basis of information technologies in the analog field is precisely the continual LA calculus: Lukasiewicz's infinite-valued logic [6], continuous logic with all its variants and generalizations, additive-

multiplicative logic (AM) algebra, predicate selection algebra, equivalence algebra and others. They determined the continual biologically inspired stage of development of LA-calculus and a new, more energy-efficient, direction of building models and their hardware implementations of artificial intelligence. Many logics are based on multi-place, multi-input operations: **min** (x_1, x_2,… x_n) and **max** (x_1, x_2, …. x_n), when defining variables on a unit interval: x_i belongs [0,1]. The image processing algorithms, basic procedures of composition-decomposition and fuzzy inference in artificial neural-fuzzy systems are also based on such multi-input min-max operations. Therefore is an urgent need to improve the hardware implementations of nodes, that perform these and similar operations. Efficiency increasing of computer systems of speed images processing that operate with arrays consists in the use of special mathematical support. The special place among such methods occupies the class of the nonlinear methods and algorithms that carried out transformation of kind: $\mathbf{B}=\{b_{ke}\}=\mathbf{F}(\mathbf{A})=\{\mathbf{\Phi}_{kl}(\mathbf{A}_{kl})\}$, where $\mathbf{\Phi}_{kl}(\mathbf{A}_{kl})$ – nonlinear function, which is determined by subset of rank and (or) index statistician of selection. It is formed by signal samples from some neighboring of this element in the sequence of the well-organized samples of signal, and it is named as variational series. By virtue of the last this subclass was adopted by rank algorithms. The algorithms of extreme filtration, using values of minimum and maximum on samples of neighborhood space, are the special cases of the rank algorithms. Any r-th index statisticians $v_s(\mathbf{r})$ of display (k, l) the set neighboring of which form other (N_s-1) the elements of selection it is possible to bind to the local histograms of distributing of values of neighboring elements and with the proper functions of the well-organized choice $F_n^m \vec{x}$ ($\vec{x}$) element, where $\vec{x}$ =(x_1, x_2, …. x_n). Such functions at any values of changing variables choose that size which at the location all right not decreasing are occupied by m-th place. These functions can be represented by a logical formula:

$$F_n^m(x)=\max_{1\le i,<\ldots.<i_{n-m+1}\le n}[\min(Xi_{1,\ldots.}Xi_{n-m+1})], \qquad \text{or } f^{(r)}(x_1,\ldots.x_n)=x^{(r)}, r=\overline{1,n},$$

where r-rank of the base operations of continuous logic (CL). Index operations are used with operations of denial, addition. The algebra, formed in a number of C = [0, 1] with base operations f(r) and (-) is named ordering Boolean algebra. The row of specific laws is inherent to it: tautology, commutative, distributive. Rank algorithms are locally-adaptive on the same essence: simplicity of local adaptation, invariance to spatial links and to signals dimension, almost algorithms complication independence from the sizes of neighboring. Also, at calculation of rank statistician and derivative

the simplifications related to informative surplus of images are possible. Sorting algorithms have been widely researched due to the need for sorting in many applications. In paper [5] approaches to creation of programmable relational optoelectronic time-pulse coded processors as base elements for sorting were shown. But in such a relational processor, working with analog signals both amplitude-coded and time-pulse-coded, the sorting structure for ordering signals is complex, since the number of base cells in the layer and the required number of layers increase proportionally with the number of input variables. Therefore, the aim is to simplify the sorting node of analog variables to build on its basis the relational processors of nonlinear image processing. The latter can be used as multifunctional nodes of ordinal logic, extremum selectors, data ordering and sorting nodes, rank filters, fragment classifier recognizers, etc. To create fully parallel algorithms and tools for morphological image processing, especially for implementing such basic operations as dilation, erosion, opening, closing, etc., the above mentioned min-max operations on sets of signals are also necessary, which represent structural windows or selected fragments processed images. Many of the morphological operations need to be repeated many times and for all the fragments of the image being processed, therefore, there is an urgent need to reduce the execution time of min-max operations and ranking operations. Consequently, the **aim of our work is design and modeling** rank analogue pre-processor for image nonlinear processing based on iterational sorting node using of CL base cells (BC) based on current mirrors (CM) with functions of preliminary analog, mixed processing.

Presentation of the main material. Structure of nonlinear processing relational preprocessor based on iterative sorting node is shown in Fig. 1. Iterative sorting node is implemented on a modification of the wave structure known from work [5], which is based on basic nodes consisting of selector-rank disjunctive-conjunctive elements (SRDCE). Our proposed below approach, oriented to the iterative wave structure, is especially important with significant n and provides integration in the case of the requirement of a multichannel connection of such devices. Since such processors have output signals that are ranked by value and not by difference of values, by some modification they can be used to organize an additional calculation of the difference of signals having neighboring ranks. And the difference in signal values is also necessary for such a function as nonequivalence. Based on the operations of bounded difference and nonequivalence, a whole set of other continuous logic complex operations and functions are constructed. For example, early we can select one of on signals by rank using multiplexer. And now we can also form signals difference between max signal and next by order. So we can find signal that

is proportional to difference of any two signals from ordered set. Such approach allows forming output complement analog signals (Fig. 2). If one of reference level is 1, than difference between the reference and any of signals is the continuous logic complement of the analog signal.

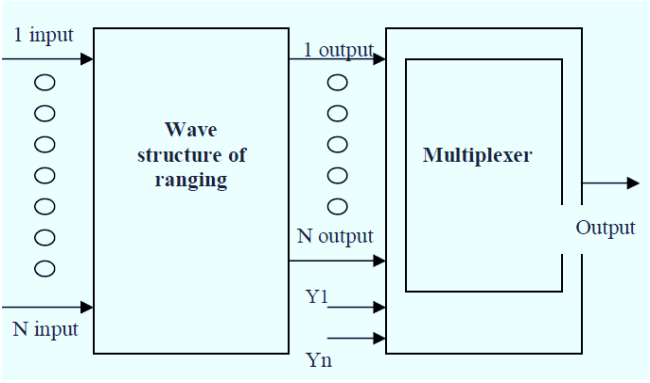

Fig. 1. Structure of nonlinear processing rank analogue preprocessor based on iterative sorting node

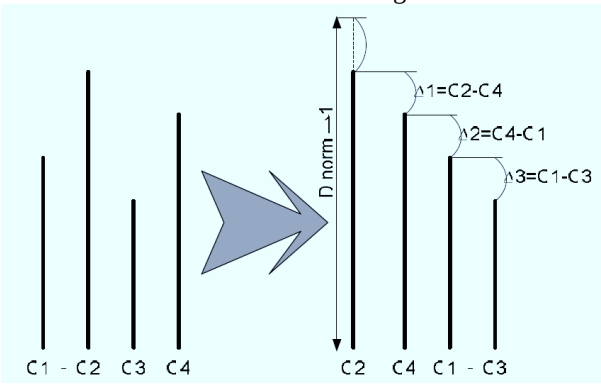

Fig. 2. Graphical representation of the processor operations

The modified iterative sorting structure based on a multichannel sampling and storage device and two linear arrays consisting of CL analog cells (disjunctive-conjunctive elements of the selector rank SRDCE with ordered outputs) is shown in Fig. 3. Fig. 4 shows the functional diagrams of these main units and their cells, which were used to model the proposed

processor structure with PSpice Orcad. The simulation results are shown in Fig. 5÷6 for different modes of operation of the iterative sorting node.

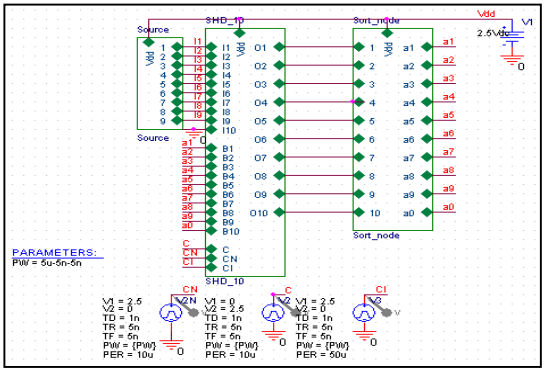

Fig. 3. The modified iterative sorting structure based on a multichannel SHD and 2 linear arrays consisting of analog SRDCE with ordered outputs.

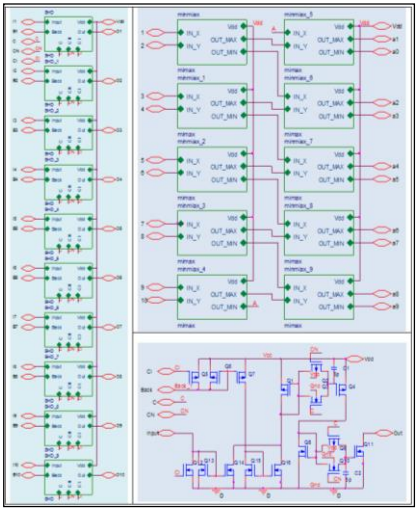

Fig. 4. Schemes of the main node of the iterative sorting structure: a multichannel SHD (left), a permutation comparison scheme as the two of linear arrays from basic CL analog cells (right above) and a 1 single channel of the sample and storage device (bottom right).

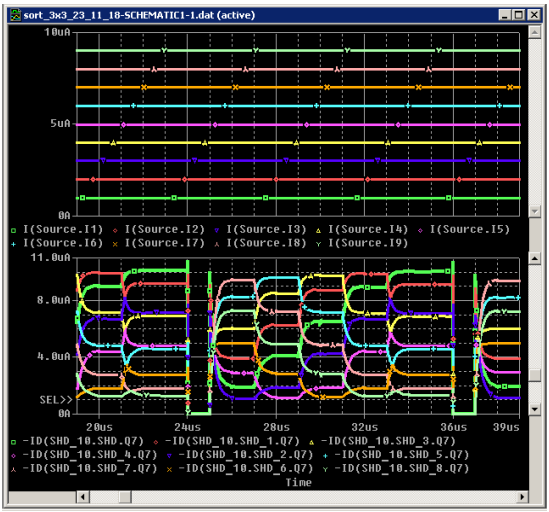

Fig. 5. Simulation results of iterative sorting structure for Vdd=2.5V, Dmax=10μA, T=12μs

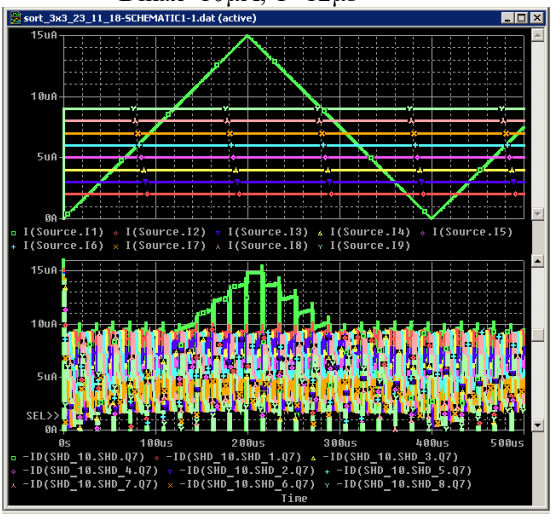

Fig. 6. Simulation results of sorting structure for Vdd=2.5V, Dmax=16μA, T=18μs in the case of one ramp / falling signal and nine constant

They show that for used 1.5μm CMOS transistors (Ts), the total sorting time of 10 signals (9 input information variables and one auxiliary) with

permissible errors does not exceed 6÷18μs (for evaluation, we take 10μs). This time is made up of the five required clocks, but the rewriting beat in the SHD and the read beat can be different. We doubled the last one and therefore the total time was proportional to 6 cycles. The levels of input signals in the figures are indicated by different colors, which allows you to see the dynamics of transitions and the change of signal levels during exchanges, permutations. At the inputs we gave signals, ordered by their levels in the reverse order.

This made it possible to more clearly demonstrate the process of ranking in which the signal with the highest level appeared at the top output of the circuit. Let us estimate the complexity of such a sorting node. Each SHD consists of 16 Ts, there are only 10. And the two lines (layers) of basic cells with min-max operations (comparisons and exchanges in essence!) consist of 10 cells, each of which is performed on 13 Ts. Therefore, the total number of transistors will be equal to: 16x10+13x10= =290.

Taking into account the presence of some other auxiliary circuits: clock signal generators, a multiplexer and matching buffers; we can assume that only up to 400 transistors will be needed. Even for the fastest and most advanced algorithms and sorting schemes, the total number of comparison and exchange operations is proportional to (nlogn)x1.5 and for n=10 is about 50.

Thus, taking into account that for the simulated circuit the power consumption was 2 mWs and Tproc = 10^{-5} s, we obtain for the simultaneous formation of ten output functions the energy efficiency estimate at the level: 500op/(10^{-5}s · 2x10^{-3}W)=25x10^{9} op / s · W. And this means that at least several hundred of them could be placed on the chip. But here the problem of interconnections will appear and the exit from it to ensure parallel inputs will be just an array of photo-detectors.

Structure of multichannel 8 bit ADC (1D array 8 bit CL_ADC) with analog signals preprocessing was described in paper[32]. It uses the same SHD, similar cells and iterative approaches, and this allows for additional in such processors to implement analogue-digital transformation, both before and after sorting the signals. The simulation results with Matcad of processing methods using the proposed preprocessor shown in Fig. 7.

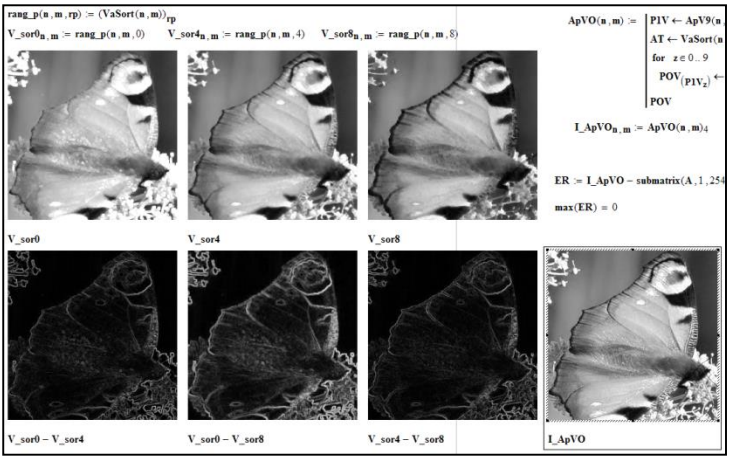

Fig. 7. The simulation results with Matcad of processing methods using the proposed image nonlinear processing preprocessor

List of literary sources

1. Fey, D., “Architecture and technologies for an optoelectronic VLSI,” Optic 112(7), 274-282 (2001).

2. Lei Yi, Guangbao Shan, Song Liu, Chengmin Xie, High-performance processor design based on 3D on-chip cache, Microprocessors and Microsystems, Volume 47, 2016, Pages 486-490, ISSN 0141-9331, http://dx.doi.org/10.1016/j.micpro.2016.07.009.

3. Krasilenko, V. G., Nikolskyy, A. I., Lazarev, A. A., "Multichannel serial-parallel analog-to-digital converters based on current mirrors for multi-sensor systems", Proc. SPIE 8550, Optical Systems Design 2012, 855022 (2013); doi:10.1117/12.2001703.

4. Krasilenko, V. G., Nikolskyy, A. I,. Lazarev, A. A., "Designing and simulation smart multifunctional continuous logic device as a basic cell of advanced high-performance sensor systems with MIMO-structure," in Photonics, Devices, and Systems VI, Dagmar Senderáková; Petr Páta; Pavel Tománek, Editors, Proc. SPIE, 9450, 94500N (2015).

5. Krasilenko, V. G., Nikolskyy, A. I,. Lazarev, A. A., Lazareva, M.V. "Design and simulation of programmable relational optoelectronic time-pulse coded processors as base elements for sorting neural networks",

Proceedings of SPIE Vol. 7723, 77231G (2010).

6. Volgin, L.I., Mishin, V.A., “Is the future digital or analog?,” Information technologies in electric power industry: Cheboksary: RESCNIT, 86-89, (1998).