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DESIGN AND MODELING OF DIGITAL MULTIFUNCTIONAL IMAGE PROCESSORS BASED ON THE SORTING NODE AND METHOD OF PROCESSING WEIGHTING-SELECTING SIGNALS OF RANK DIFFERENCES

Introduction. Advanced direction becomes fast parallel images processing using optoelectronics for interconnects and non-conventional MIMO-system, corresponding matrix logics (ML) (continuous, neural-fuzzy and others) and corresponding mathematical apparatus [1-5]. Photo-detectors can be monolithically integrated with digital electronics in silicon, which allows the realization of stacked 3-D chip architecture in principle and significantly simplifies design of OE-VLSI circuits [2]. Smart image sensors with ADC [4, 5] show a great application field and potential. Our approach favors smart pixel architecture combining parallel signal detection with parallel processing in circuit, what guarantees the fastest processing. For self-learning neural networks (NN) based on equivalency models (EM) [6, 7], the elements of MLs are required. For the description and modeling of each continual subject domain and the class of its tasks, its own logical-algebraic apparatus (LAA) is required. Formal LAA is based on clear rules that allow you to make an exact description of a certain class of problems and even suggest an algorithm for solving them. The basis of information technologies in the analog field is precisely the continual LAAs: infinite-valued logic [8], continuous logic with all its variants and generalizations, additive-multiplicative logic (AM) algebra, predicate selection algebra, equivalence algebra [6-7]. They determined the biologically inspired stage of development of LAAs and new more energy-efficient direction of models and hardware implementations of artificial intelligence. Many logics are based on multi-input operations **min** ($x_1, x_2,\dots x_n$) and **max** ($x_1, x_2, \dots. x_n$). The image processing algorithms, basic procedures of composition-decomposition, fuzzy inference in artificial neural-fuzzy systems are also based on multi-input min-max operations. Therefore is an urgent need to improve the nodes, that perform these and similar operations. Efficiency increasing of systems of speed images processing in the use of special mathematical support. The special place among such methods occupies the class of the nonlinear algorithms that carried out transformation of kind: $\mathbf{B}=\{b_{ke}\}=\mathbf{F}(\mathbf{A})=\{\mathbf{\Phi}_{kl}(\mathbf{A}_{kl})\}$, where $\mathbf{\Phi}_{kl}(\mathbf{A}_{kl})$ — nonlinear function, which is determined by subset of rank and (or) index statistician of selection. By virtue of the last this subclass was adopted by rank algorithms.

The algorithms of extreme filtration, using values of **min** and **max** on samples of neighborhood space, are the special cases of the rank algorithms. Any r-th index statisticians $v_s(\mathbf{r})$ of display (k, l) the set neighboring of which form other (N_s-1) the elements of selection it is possible to bind to the local histograms of distributing of values of neighboring elements and with the proper functions of the well-organized choice $F_n^m \vec{x}$ ($\vec{x}$) element, where $\vec{x}$ =(x_1, x_2, …. x_n). Such functions at any values of changing variables choose that size which at the location all right not decreasing are occupied by m-th place. These functions can be represented by a logical formula:

$$F^{(r)}(x_1,\ldots x_n)=x^{(r)}, r=\overline{1,n},$$

where r-rank of the base operations of continuous logic (CL). Thus for r = n this operation passes to n-local disjunction, for r=1 to n-local conjunction. The algebra formed in a number of C = [0, 1] with base operations f(r) and complementarity operation (-) is named ordering Boolean algebra. Rank algorithms are locally-adaptive on the same essence: simplicity of local adaptation, invariance to spatial links and to signals dimension, almost algorithms complication independence from the sizes of neighboring. Sorting algorithms have been widely researched due to the need for sorting in many applications. In paper [9] approaches to creation of programmable relational processors for sorting were shown. But in such a relational processor, working with analog signals, the sorting structure for ordering signals is complex. Therefore, the aim is to simplify and digitize the sorting node to build on its basis the relational processors of nonlinear image processing. The latter can be used as nodes of ordinal logic, data ordering and sorting nodes, rank filters, fragment classifier recognizers, as tools for morphological operations as dilation, erosion, opening, closing. The above mentioned min-max operations on sets of signals are also necessary, which represent structural windows or selected fragments processed images. Many of the morphological operations need to be repeated many times and for all the fragments of the image being processed, therefore, there is an urgent need to reduce the execution time of min-max operations and ranking operations. Therefore, the **goal of our work** is to search new options for implementing both signal sorting nodes, including digital, providing increased accuracy and speed, and based on them relational non-linear image processing processor with advanced functionality. In addition, taking into account the recent emergence of a new element base, our task is to prove the possibility of creating on the FPGA, practically in one chip, an image preprocessor (IP) with enhanced technical characteristics and a wide range of commands through the use of a new method of processing pre-ranked signals and (or) their differences. To achieve this goal, it is necessary to simulate the algorithms and methods themselves, and then based on

them design and simulate the technical options for the implementation of non-linear IP and their main nodes.

Presentation of the main material. Our proposed allows ranking of signals and forming output signals are shown in Fig. 1. Structure of digital multifunctional image processor (DMIP) DMIP_2 based on FPGA with serial input and registers memory to form a vector of signals to be sorted and 1 output using sorting unit (SU) based on modified conveyor homogeneous wave structure (MCHWS) consisting of layers of digital comparison switching circuits is shown in Fig.2. Here variant DMIP_1 with 10 inputs and 1 output and supply of all input signals in parallel is not shown. For the convenience of data input, we have developed and modeled a processor DMIP_2 circuit with register memory for fast sequential image input and automatic sequential search of processed windows. It is shown in Fig. 2. Simulation results of DMIP_2 are shown in Fig. 3, 4.

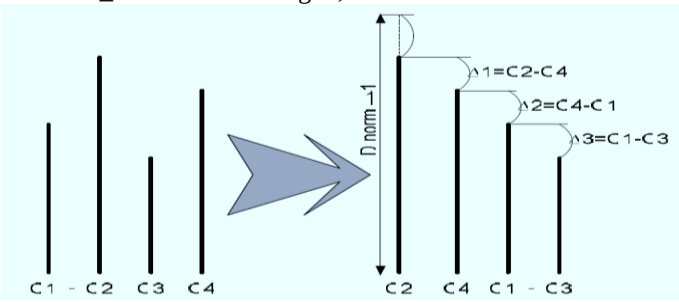

Fig. 1. Graphical representation of the processor operations of ranking

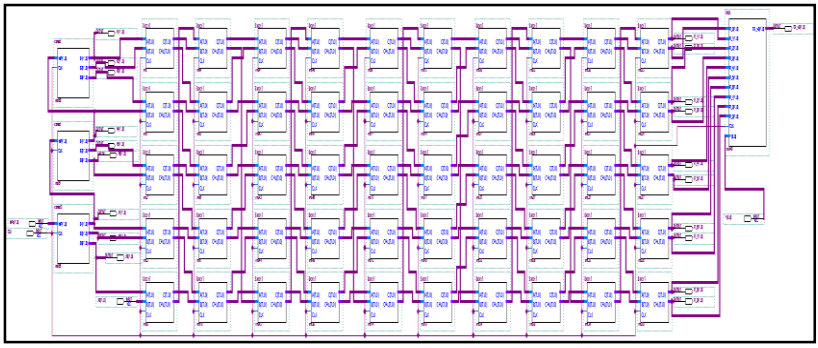

Fig. 2. FPGA Structure of DMIP_2 with serial input and registers memory to form a vector of signals to be sorted and 1 output

Since such processor have output signals that are ranked by value and not by difference of values, by some modification [9] they can be used to organize an additional calculation of the difference of signals having neighboring ranks. Besides, the difference in signal values is also necessary for such a function as nonequivalence. Based on the operations of bounded difference and nonequivalence, a whole set of other continuous logic complex operations and functions are constructed. For example, early we can select one of n signals by rank using multiplexer. There is only 1 output (ranks). And now we can also form signals difference between max signal and next by order. So we can find signal that is proportional to difference of any two signals from ordered set. Such approach allows to formed output complement signals. If one of reference level is D=1 (255), than difference between the reference and any of signals is the complement of the signal. Therefore, we will develop this idea further, taking into account the fact that the selection, amplification, weighting and addition of signals are simple.

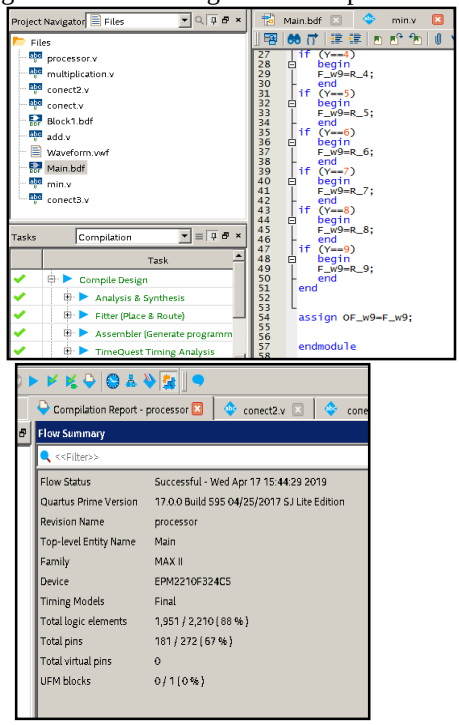

Fig. 3. Simulation of DMIP_2 based on FPGA (window fragments)

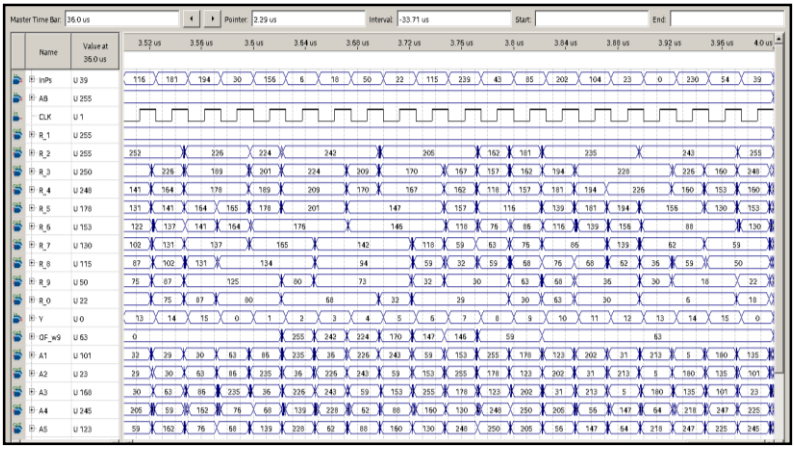

Fig. 4. Simulation results of DMIP_2 based on FPGA with serial input and registers memory and 1 output (issuing ranks, one switch)

The simulation results of DMIP_3 (Fig. 5) with serial input and registers memory, 2 outputs for rank and rank differences signals weighing-selection processing are shown in Fig. 6-10.

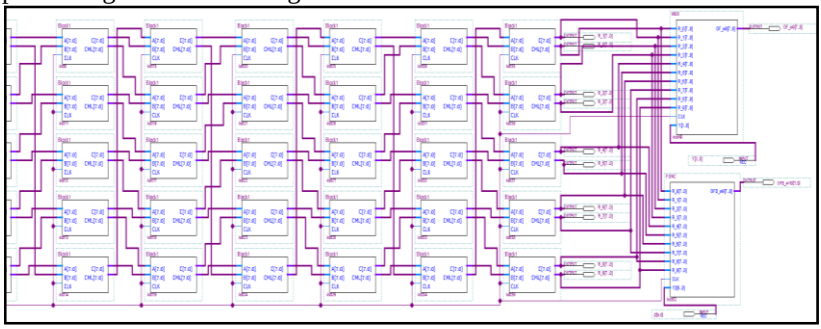

Fig. 5. Structure of DMIP_3 based on FPGA with serial input and registers memory to form a vector of signals to be sorted, 2 outputs for rank and rank differences signals weighing-selection processing

As can be seen from Fig. 3, 4, 6, 7 the resources of the Altera FPGA chip EP3C16F484 Cyclone III family are not fully used in the first case, and in the second for the processor with register memory and two outputs almost completely (there is a small margin).

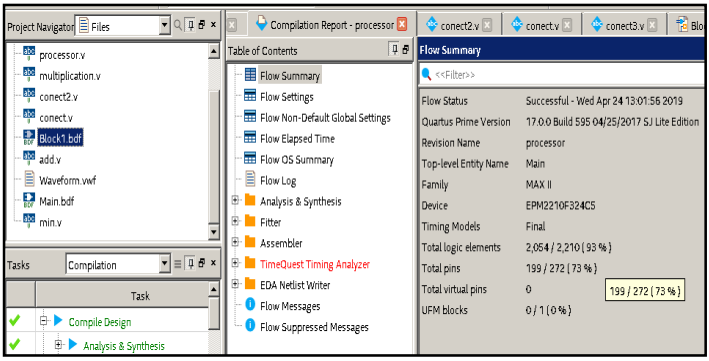

Fig. 6. Simulation of DMIP_3 based on FPGA with serial input and 2 output (window fragments)

The processing cycle in the pipelined structure of DMIP and SU did not exceed 25 nanoseconds, which makes it possible to achieve an input / output rate of pixels of the processed and processed images at the level of 40MHz. During the processing cycle, DMIP_1 essentially performs (9 * ln9-estimates for the best algorithms!) Sorting operations and generates all the ranks and their differences, which gives, taking into account the wide variety of output functions, performance estimates of at least 10^9 operations per second.

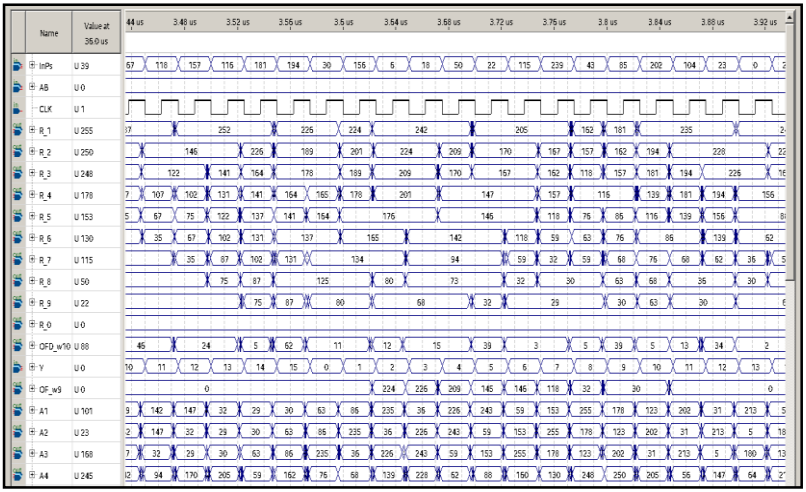

Fig. 7. Simulation results of DMIP_3 with 2 outputs (issuing ranks, two switches) in case of formation of a difference of ranks r2-r3

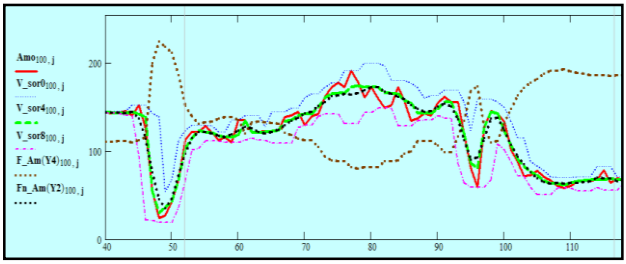

Fig. 8. A good example of image line processing using proposed DMIP: Original line (red) and received rank and other output functions.

Conclusions. We show the results of design the new FPGA-DMIPs with digital accuracy. Calculations show that in the case of using Altera FPGA chip EP3C16F484 of Cyclone III family, it is possible to implement DMIP for image size of 64*64 and window 3*3 in the one chip.

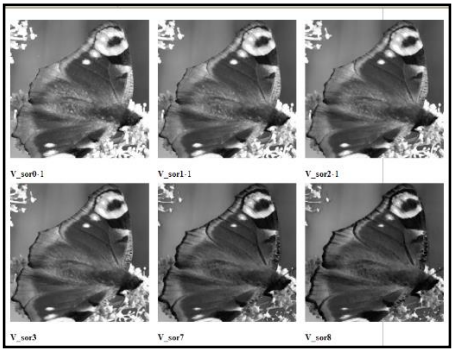

Fig. 9. The results of image transformations with DMIP for different rank : 0, 1, 2, 3, 7, 8, respectively.

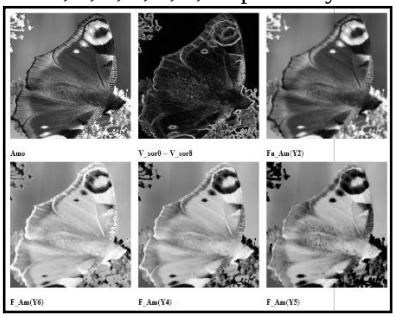

Fig. 10. The results of the Amo image transformations using DMIP for different rank values and different functions defined by the control vector Y

For 2.5V and clock frequency of 200MHz the power consumption will be at the level of 200mW and the calculation time for pixel of filters will be 25ns.

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